MODULE 4

Fundamentals of Sequential Design and Design of Advanced Sequential Machines

Structure

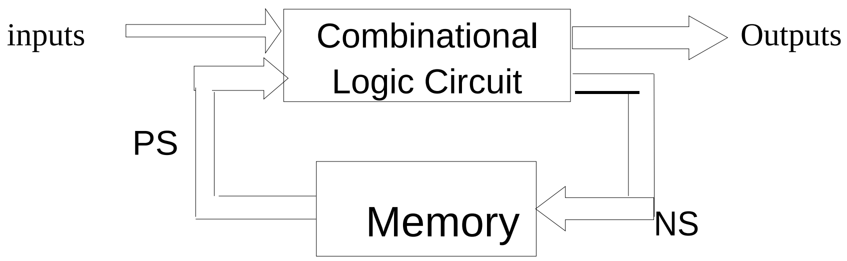
4.1 Objevtive

- To know about different models of a system and differentiate between them
- Designing of sequential circuit
- Designing of sequential circuit based on problem statement

4.2 Introduction

Definition :

In sequential networks, the outputs are function of present state and present external inputs. Present state simply called as states or past history of circuit. The existing inputs and present state for sequential circuit determines next state of networks.



Model of Sequential Network

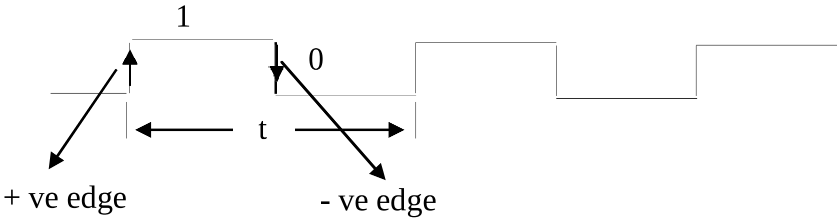
Types of Sequential Network :

1. **Asynchronous Sequential Network :** The changes in circuit depends on changes in inputs depending on present state. But the change in memory state is not at given instant of time but depending on input.
2. **Synchronous Sequential Network :** Output depends on present state and present inputs at a given instant of time. So timing sequence is required. So memory is allowed to store the changes at given instant of time.

Structure and Operation of Clocked Synchronous Sequential Circuit :

In synchronous sequential circuit, the network behavior is defined at specific instant of time associated with special timing. There is master clock which is common to all FFs that is used in memory element. Such circuits are called as clocked synchronous sequential circuit.

Clock : Clock is periodic waveform with one positive edge and one negative edge during each period.



This clock is used for network synchronization

<u>Basic Operation of Clocked Synchronous Sequential Circuit</u>

Q indicates all present state of FF.

Q+ indicates next state of FF in

network. X indicates all external

inputs.

Q+ = f(x,Q) This is next state of network.

Z indicates output signal of sequential networks.

Z = g(X,Q)

4.3 Mealy and Moore models

The structure shown in given figure is called as <u>Mealy Model or Mealy Machine.</u>

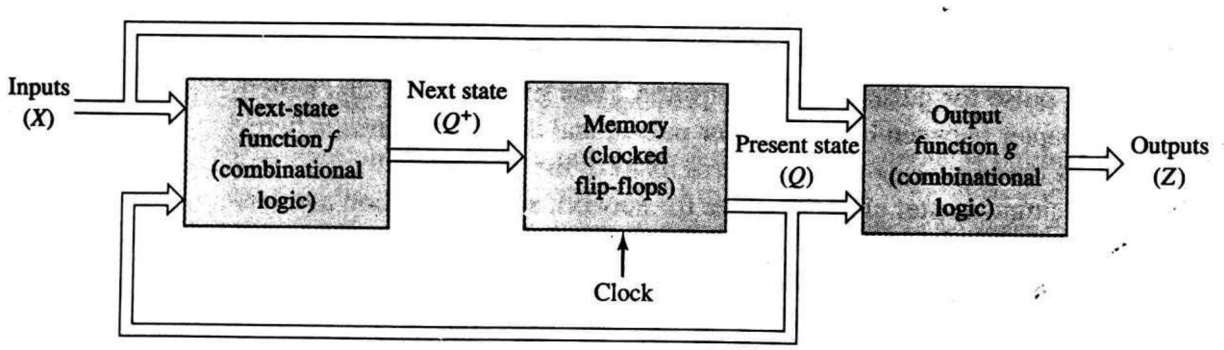


Figure 7.3 Mealy model of a clocked synchronous sequential network.

There are two types of finite state machines that generate output −

- Mealy Machine
- Moore machine

Mealy Machine

A Mealy Machine is an FSM whose output depends on the present state as well as the present input.

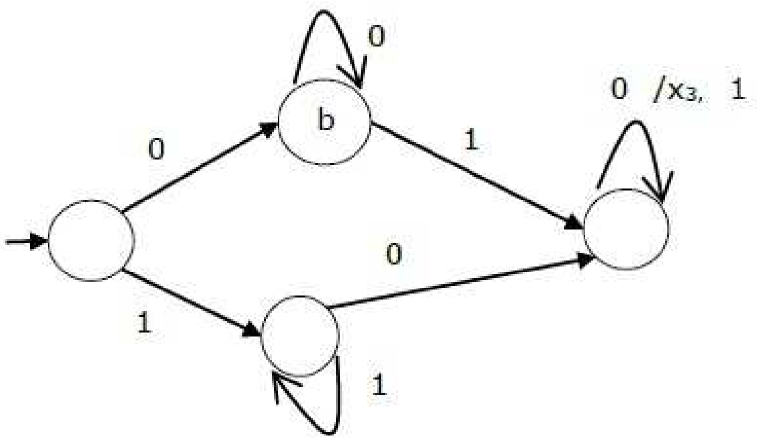
It can be described by a 6 tuple (Q, ∑, O, δ, X, q_0) where −

- **Q** is a finite set of states.
- ∑ is a finite set of symbols called the input alphabet.
- **O** is a finite set of symbols called the output alphabet.
- **δ** is the input transition function where δ: Q × ∑ → Q
- **X** is the output transition function where X: Q × ∑ → O
- **q_0** is the initial state from where any input is processed (q_0 ∈ Q).

The state table of a Mealy Machine is shown below −

Present state	Next state			
	input = 0		input = 1	
	State	Output	State	Output
→ a	b	x_1	c	x_1
b	b	x_2	d	x_3
c	d	x_3	c	x_1
d	d	x_3	d	x_2

The state diagram of the above Mealy Machine is −



Moore Machine

Moore machine is an FSM whose outputs depend on only the present state.

A Moore machine can be described by a 6 tuple (Q, ∑, O, δ, X, q_0) where −

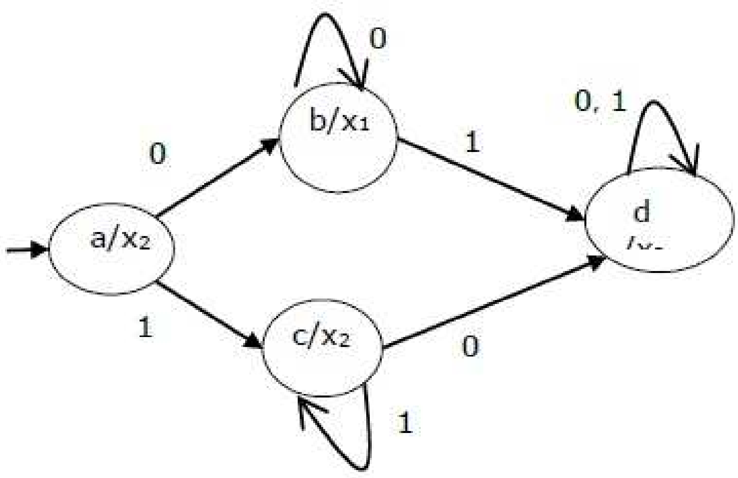
- **Q** is a finite set of states.
- ∑ is a finite set of symbols called the input alphabet.
- **O** is a finite set of symbols called the output alphabet.
- **δ** is the input transition function where δ: Q × ∑ → Q
- **X** is the output transition function where X: Q → O
- $\mathbf{q_0}$ is the initial state from where any input is processed (q_0 ∈ Q).

The state table of a Moore Machine is shown below −

Present state	Next State		Output
	Input = 0	Input = 1	
→ a	b	c	x_2
b	b	d	x_1

c	c	d	x_2
d	d	d	x_3

The state diagram of the above Moore Machine is −

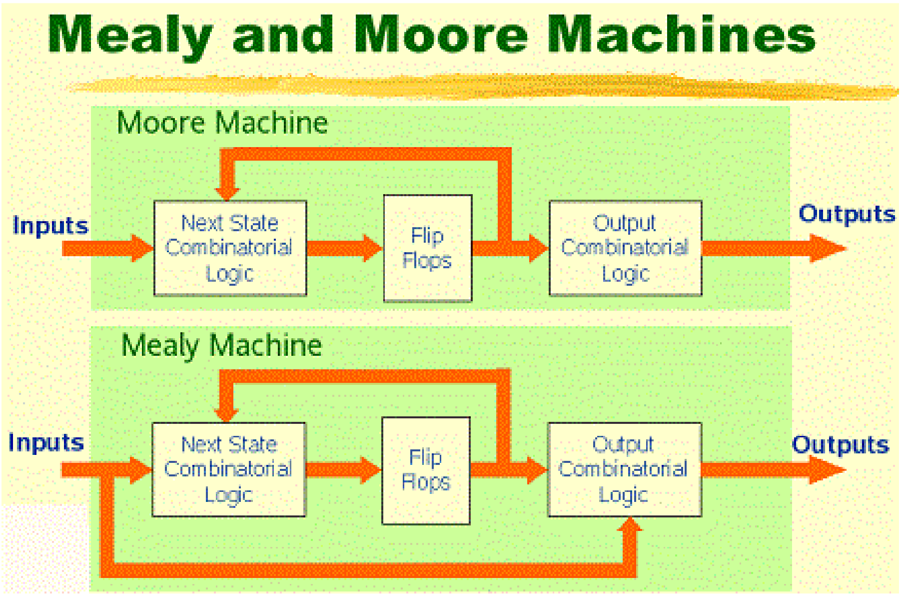


Mealy Machine vs. Moore Machine

The following table highlights the points that differentiate a Mealy Machine from a Moore Machine.

Mealy Machine	Moore Machine
Output depends both upon present state and present input.	Output depends only upon the present state.
Generally, it has fewer states than Moore Machine.	Generally, it has more states than Mealy Machine.
Output changes at the clock edges.	Input change can cause change in output change as soon as logic is done.

Mealy machines react faster to inputs	In Moore machines, more logic is needed to decode the outputs since it has more circuit delays.



Block Diagram of Mealy and Moore Machines

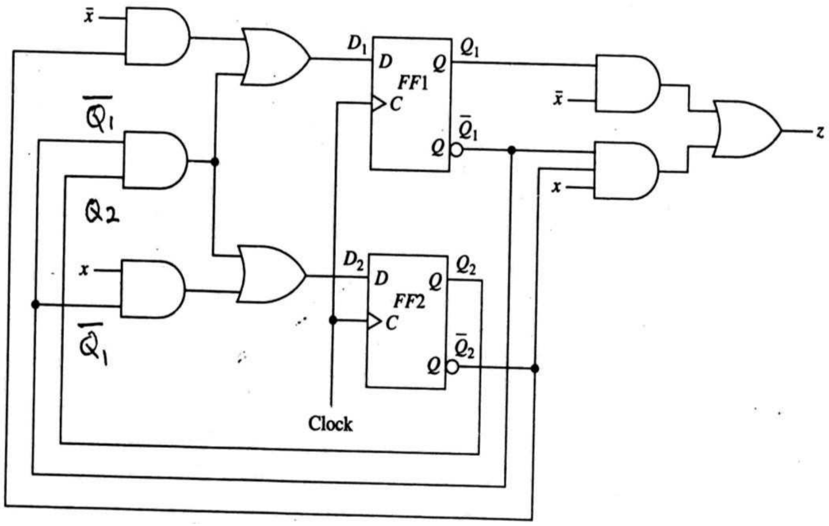
Difference between Mealy Model and Moore Model of Synchronous Sequential Circuit

Mealy Model : In Mealy Model the next state is function of external inputs and present state. The output is also function of external inputs and present state. The memory state changes with master clock.

$Q+ = f(X,Q)$ $\quad\quad$ $Z = g(X,Q)$

Moore Model : In Moore Model the next state is function of external inputs and present state. But the output is function of present state. It is not dependent on external inputs. The no. of FFs required to implement circuit is more compared with Mealy Model,

$Q+ = f(X,Q)$ $\quad\quad$ $Z = g(Q)$

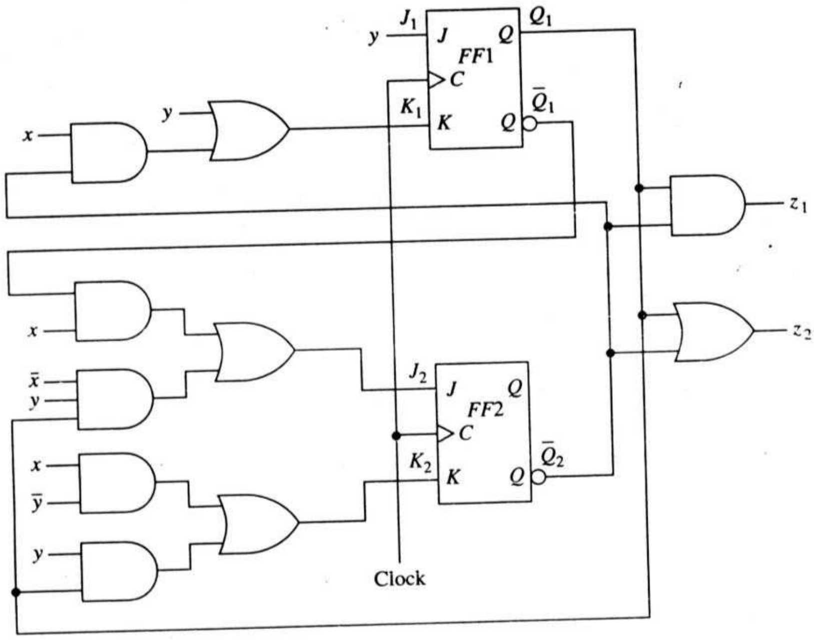


Logic Diagram for Mealy Network

$$D1 = \overline{xQ2} + \overline{Q1Q2}$$

$$D2 = x\overline{Q1} + \overline{Q1}Q2$$

$$Z = \bar{x}Q1 + Q1\,Q2\,x$$



Logic Diagram for Moore Network

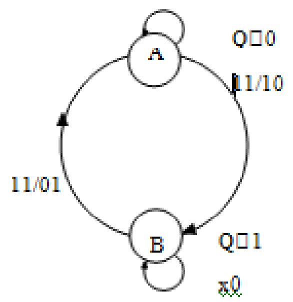
Transition Tables :

Instead of using algebraic equations for next state and outputs of sequential network, it is more convenient and useful to express the information in tabular form. The Transition Table or State Transition Table or State Table is the tabular representation of the transition and output equations. This table consist of Present State, Next State, external inputs and output variables. If there are n state variables then 2n rows are present in state table.

4.4 State machine notation

Input Variables : External input variables to sequential machine as inputs.
Output Variables : All variables that exit from the sequential machine are output variables.
State : State of sequential machine is defined by the content of memory, when memory is realized by using FFs.
Present State : The status of all state variable i.e. content of FF for given instant of time t is called as present state.
Next State : The state of memory at t+1 is called as Next state.
State Diagram : State diagram is graphical representation of state variables represented by circle. The connection between two states represented by lives with arrows and also indicates the excitation input and related outputs.
Output Variables : All variables that exit from the sequential machine are output variables.

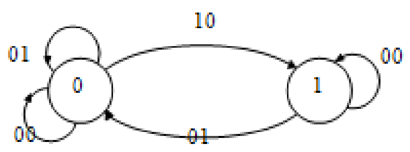
4.5 synchronous sequential circuit analysis and design.



State diagram of J-K FF

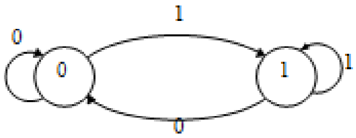
Application Table of JK FF

PS	NS	FF input	
Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



State diagram of SR FF

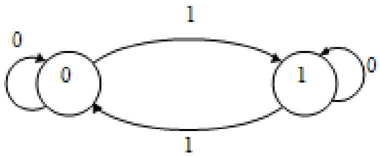
PS	NS	FF i/p	
Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



State diagram of D FF

Application Table of D FF

PS	NS	FF i/p
Q	Q+	D i/p
0	0	0
0	1	1
1	0	0
1	1	1



State diagram of T FF

Application Table of FF

PS	NS	FF i/p
Q	Q+	T i/p
0	0	0
0	1	1
1	0	1
1	1	0

Transition table for Mealy Network

Present state (Q_1Q_2)	Next state ($Q_1^+Q_2^+$)		Output (z)	
	Input (x)		Input (x)	
	0	**1**	**0**	**1**
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

$Q_1^+ = \overline{x}\overline{Q_2} + \overline{Q_1}Q_2$, $\quad Q_1^+ = D_1$

$Q_2^+ = x\overline{Q_1} + \overline{Q_1}Q_2$, $\quad Q_2^+ = D_2$

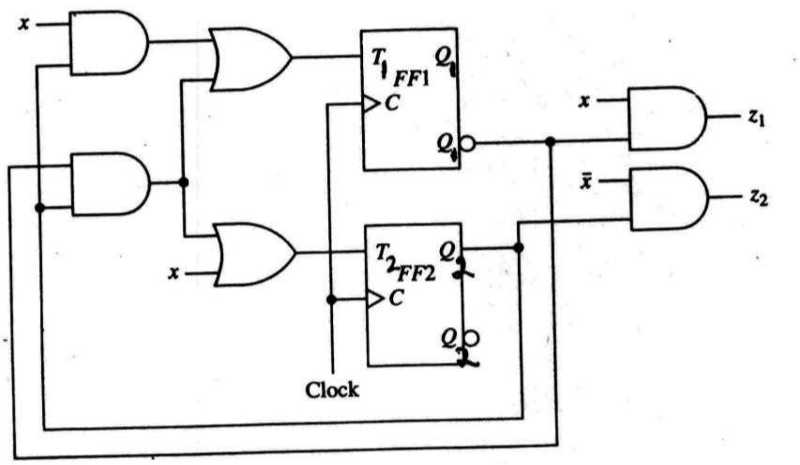
$Z = \overline{x}Q_1 + \overline{Q_1}\,\overline{Q_2}x$

Transition table for Moore Network

PS(Q1Q2)	NS(Q1+,Q2+)				O/p (Z1Z2)
	I/p XY				
	00	01	10	11	
00	00	10	01	11	01
01	01	11	00	11	00
10	10	01	00	00	11
11	11	00	10	00	01

$$Z_1 = \overline{Q_2}Q_1 \, , Z_2 = Q_1 + \overline{Q_2}, \quad J_1 = y$$

$$K_1 = \overline{Q_2}x + y, \; J_2 = \overline{Q_1}\,\mathrm{x} + \overline{\mathrm{x}}\mathrm{y}Q_1 \, , K_2 = x\overline{y} + y\overline{Q_1},$$



Synchronous Sequential Circuit

$$T_1 = xQ_2 + \overline{Q_1}Q_2, \quad Q_1^{\;+} = T_1 \oplus \mathrm{Q}_1$$

$$T_2 = x + \overline{Q_1}Q_2 \, , \quad Q_2^{\;+} = T_2 \oplus \mathrm{Q}_2$$

$$Z_1 = x\overline{Q_1}, \quad Z_2 = \overline{\mathrm{x}}Q_2$$

4.6 Construction of state Diagrams

State Tables :

State table consist of PS, NS and output section. The PS and NS of state tables are obtained by replacing the binary code for each in the transition table by newly defined symbol. The output section is identical to output section of transition table.

Symbols for state can be S1, S2, S3,……Sn or A, B, C, D, E….

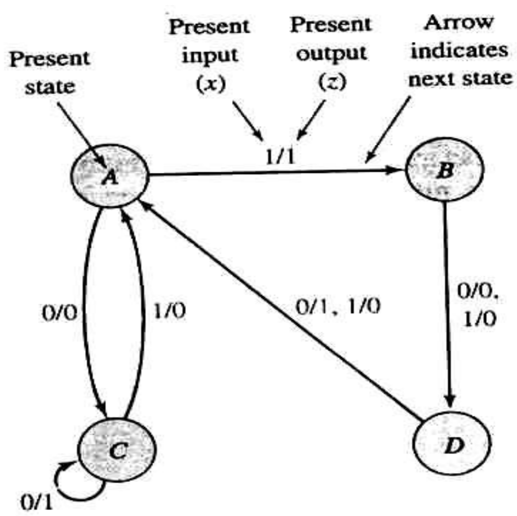
State table for Mealy Machine

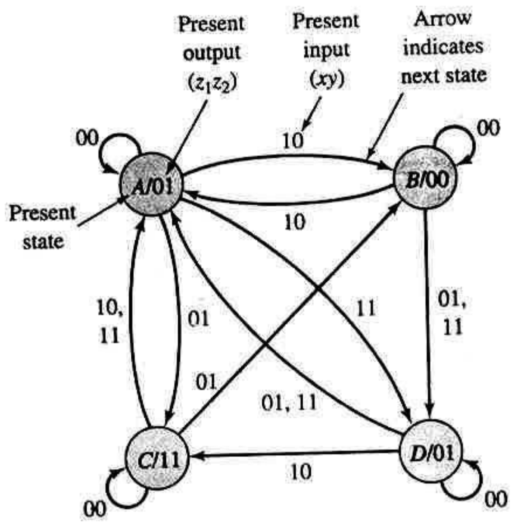
PS	NS		O/p Z	
00 – A	C	B	0	1
01 – B	D	D	0	0
10 – C	C	A	1	0
11 – D	A	A	1	0

State Diagram :

It is graphical representation of state tables. Each state of network is represented by labeled node.

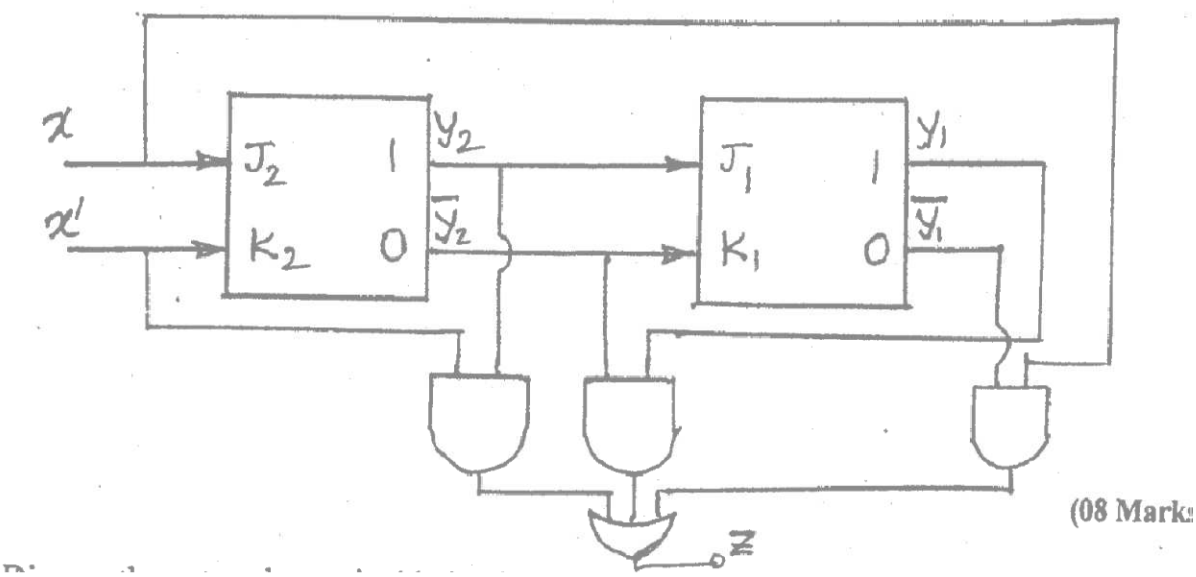
Directed branches connect the nodes to indicate transition between states. The directed branches are labeled according to the values of external input variable that permit transition. The output of sequential network is also entered in state diagram. In case of Moore Network state diagram, thE values of input for output is not written.





State diagram for Mealy Network

P1:



Analysis of Synchronous Circuit

The given circuit in above figure is Mealy Network and the output is function of input variable and PS of FF. The analysis of above circuit is as follows.

The Excitation and Output Function

$$Z = \overline{x}y_2 + y_1\overline{y_2} + x\overline{y_1}$$

$$J_2 = x, \quad K_2 = \overline{x}, \quad J_1 = y_2, \quad K_1 = \overline{y_2}$$

By substituting the FF inputs in characteristic equation, the next state of FF is obtained in terms of PS of FF and external input.
The characteristic equation of JK FF is

$$Q^{+} = J\overline{Q} + \overline{K}Q$$

$$Q_1^{+} = J_1\overline{Q_1} + \overline{K_1}Q_1 = Q_2$$
$$Q_2^{+} = J_2\overline{Q_2} + \overline{K_2}Q_2 = x$$

The Excitation Table

PS Q2 Q1 (y2 y1)	Excitation input J2 K2 x=0, 1	J1 K1 x=0, 1	Output Z x=0, x=1
0 0	0 1	0 1	1 1
0 1	0 1	0 1	0 0
1 0	0 1	1 0	1 1
1 1	0 1	1 0	2 0

$J_1 = y_2 = Q_2,\ \ K_1 = \overline{y_2} = \overline{Q_2}$
$J_2 = x,\ \ K_2 = \overline{x},\ \ Z = \overline{x}y_2 + \overline{y_2}\,\overline{y_1} + x\overline{y_1}$
When $x = 0,\ z = y_2 + \overline{y_1}$ *and When* $x = 1,\ \ z = \overline{y_1}$

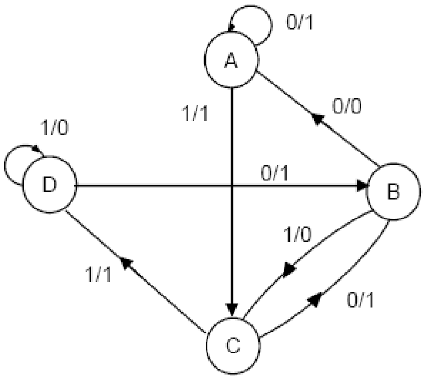
State Table

PS			NS						O/p Z	
			x = 0			x = 1				
Q2 (y2)	Q1 (y1)	state	Q2+	Q1+	state	Q2+	Q1+	state	X=0	X=1
0	0	A	0	0	A	1	0	C	1	1
0	1	B	0	0	A	1	0	C	0	0
1	0	C	0	1	B	1	1	D	1	1
1	1	D	0	1	B	1	1	D	1	0

Q1+ = Q2 = y2
Q2+ = x

$$if\ \ x = 0,\ z = y_2 + \overline{y_1}$$
$$if\ \ x = 1,\ \ z = \overline{y_1}$$

State diagram



ABCD Represnts present state

4.7 Outcome

- **Will know difference between Milley and Moore model type of sequential circuits**
- **To write state diagram for sequential circuit or vice versa.**

4.9Future Readings

http://nptel.ac.in/courses/117105080/

https://www.youtube.com/watch?v=VnZLRrJYa2I

"Logic Design" by RD Sudhaker Samuel

"Digital Logic Applications and Design" by John M Yarbrough, 2011 edition