MODULE-2: Field Effect Transistors (FET)

Definition:
FET is a three terminal electronic device used for variety of applications that match with BJT. In FET, an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between controlling and controlled quantities. In a Field effect device current is controlled by the action of an electron field, rather than carrier injection.

The main difference between BJT and FET is BJT is a current controlled device while FET is a voltage controlled device. This is shown in fig 1.

![Fig 1: Comparison between BJT and FET](image)

**TYPES OF FETS:**
1. Junction Field Effect Transistors (JFETs)
2. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

**JUNCTION FIELD EFFECT TRANSISTORS (JFETS):**
JFET is a unipolar device as conduction in the device is dependent on either electrons or holes. Accordingly there are two types of JFET; namely: n-Channel JFET and p-Channel JFET.

**Features of FET:**
- FET is a voltage controlled device.
- FET is a unipolar device.
- FET has high input impedance
- AC voltage gain of JFET is low
- FET has higher temperature stability.
- FET are small in size and hence are useful in ICs.

**CONSTRUCTION AND CHARACTERISTICS OF N-CHANNEL JFET:**
The basic construction of the n-channel JFET is as shown in fig 2. The major part of the structure is the n-type material which forms the channel between embedded layers of p-
type material. The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), whereas the lower end of the material is connected through an ohmic contact referred to as source (S). The 2 p-type materials are connected together to the gate (G) terminal. In the absence of any applied potentials, JFET has 2 p-n junctions under no bias condition. As a result, depletion region is formed at each junction.

**OPERATION:**

Fig 3 shows the working of n-channel JFET for different gate-source voltage ($V_{GS}$) and drain to source voltage ($V_{DS}$) = 0V.

- **Case i: $V_{GS} = 0$ and $V_{DS} = 0$**
Under zero bias condition depletion region around the p-n junction is thin and thus exhibits low channel resistance.

Case ii: $V_{GS} = 0$ and $V_{DS} = +$ small voltage.

The gate and source are at the same potential and the instant the voltage $V_{DS}$ is applied the electrons in the n-channel are drawn towards the drain terminal establishing drain current ($I_D$).

Due to reverse biasing of the p-n junction for the length of the channel results in gate current = 0.

As $V_{DS}$ is increased further, the drain current increases. When $V_{DS} = V_P$, the depletion region widens causing reduction in the channel width. The reduced path of conduction causes the resistance to increase and the current saturates. When $V_{DS}$ is further increased, the two depletion regions touch resulting in pinch-off condition. The drain characteristics (plot of $I_D$ vs $V_{DS}$ for $V_{GS} =$ constant is as shown in fig 4.

Case iii: $V_{GS} =$ -ve voltage and $V_{DS} = +$ small voltage.

The effect of applied reverse bias on gate and source widens the depletion regions around the p-n junctions but at the lower levels of $V_{DS}$. The resulting saturation level for $I_D$ is reduced and will continue to decrease as $V_{GS}$ is made more and more negative. The drain characteristics is as shown in fig 5 for different values of $V_{GS}$. When $V_{GS} = -V_P$, pinch-off condition occurs resulting in $I_D = 0$. $V_P$ is called pinch-off voltage.

The region to the left of pinch off locus is called ohmic region and the region to the right of pinch-off locus is saturation region. This region of JFET is employed for linear amplifiers. In ohmic region JFET can be employed as a variable resistor. The resistance is controlled by $V_{GS}$. As $V_{GS}$ becomes more and more negative, the slope of the characteristics becomes more and more horizontal indicating increasing resistance level.

The resistance is given by the equation 1.

![Diagram](image1.png)
Fig 5: Drain characteristics of JFET for different $V_{GS}$ values.

TRANSFER CHARACTERISTICS OF N-CHANNEL JFET:

Transfer characteristics are a plot of $I_D$ as a function of $V_{GS}$ with $V_{DS}$ as constant. Shockley Equation as in equation 1 is used to plot transfer characteristics.

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$  \hspace{1cm} Eqn (1)

$I_D$ depends on $V_{GS}$ in a non-linear manner. As a result, FET’s are often referred to square law devices. Using the drain characteristics on the right of Y-axis, we can draw a horizontal line from the saturation region of the curve denoted as $V_{GS} = 0V$ to the $I_D$ axis. The resulting current level for both the graphs is $I_{DSS}$.

When $V_{GS} = V_P$, the drain current is 0mA, defining another point on transfer curve. Transfer curve is a direct transfer from input to output variables. Transfer characteristics are a parabolic curve as shown in fig 6.
Fig 6: Transfer characteristics from drain characteristics

TRANSFER CHARACTERISTICS: SHORT-HAND METHOD
Transfer characteristics can also be obtained by applying following conditions to schokley’s equation (1).

Condition 1: \( V_{GS} = 0 \)

\[
I_D = I_{DSS}
\]

Condition 2: \( V_{GS} = V_P \)

Therefore from equation 1 \( I_D = 0 \text{mA} \).

Condition 3: \( V_{GS} = V_P/2 \)
Therefore from equation 1, \( I_D = I_{DSS}(1 - \frac{1}{2})^2 \)

\[
I_D = I_{DSS}/4
\]

Condition 4: \( I_D = I_{DSS}/2 \)
From eq(1), \(V_{GS} = VP(1 - \sqrt{ID/IDSS})\)

\[
V_{GS} = VP(1 - \sqrt{0.5}) \\
V_{GS} = 0.3VP
\]

Points are marked for these conditions of \(V_{GS}\) and \(ID\) and the co-ordinates are joined using smooth curve.

**CONSTRUCTION AND CHARACTERISTICS OF P-CHANNEL JFET:**

The basic construction of the p-channel JFET is as shown in fig 2. The major part of the structure is the p-type material which forms the channel between embedded layers of p-type material. The top of the p-type channel is connected through an ohmic contact to a terminal referred to as the drain(D), whereas the lower end of the material is connected through an ohmic contact referred to as source(S). The 2 n-type materials are connected together to the gate (G) terminal. In the absence of any applied potentials, JFET has 2 p-n junctions under no bias condition. As a result, depletion region is formed at each junction.

![Fig 7 Construction of n-channel JFET](image)

**OPERATION OF P-CHANNEL JFET:**

Case i: \(V_{GS} = 0\) and \(V_{DS} = 0\)
- Under zero bias condition depletion region around the p-n junction is thin and thus exhibits low channel resistance.

**Case ii: \( V_{GS} = 0 \) and \( V_{DS} = -\text{ve small voltage} \).**

The gate and source are at the same potential and the instant the voltage \( V_{DS} \) is applied the holes in the p-channel are drawn towards the drain terminal establishing drain current (ID).

Due to reverse biasing of the p-n junction for the length of the channel results in gate current \( = 0 \).

As \( V_{DS} \) is increased further, the drain current increases. When \( V_{DS} = -V_P \), the depletion region widens causing reduction in the channel width. The reduced path of conduction causes the resistance to increase and the current saturates. When \( V_{DS} \) is further increased, the two deletion regions touch resulting in pinch-off condition. The drain characteristics (plot of ID vs VDS for \( V_{GS} = \text{constant} \) is as shown in fig 8).

**Case iii: \( V_{GS} = +\text{ve voltage} \) and \( V_{DS} = -\text{ve small voltage} \).**

The effect of applied reverse bias on gate and source widens the depletion regions around the p-n junctions but at the lower levels of \( V_{DS} \). The resulting saturation level for ID is reduced and will continue to decrease as \( V_{GS} \) is made more and more positive. The drain characteristics are as shown in fig 8 for different values of \( V_{GS} \). When \( V_{GS} = -V_P \), pinch-off condition occurs resulting in \( ID = 0 \). \( V_P \) is called pinch-off voltage.

![Fig 8: Drain Characteristics of p-channel JFET](image)

**Symbols of JFET:**
Fig 9(a) and 9 (b) shows the symbols of n-channel and p-channel FET respectively.
Fig 9: JFET Symbols.
9(a) n-Channel JFET  
9(b)p-channel JFET

**Metal Oxide Semiconductor Field Effect Transistors (MOSFETs):**

MOSFET is a type of Field Effect Transistor in which majority charge carriers flow in the channel. The width of the channel is controlled by an electrode called gate. Channel width determines how well the device conducts.

MOSFETS are useful in high-speed switching circuits and in Integrated Circuits.

There are two types of MOSFET's:

(i) Depletion type MOSFET  
(ii) Enhancement type MOSFET

**DEPLETION TYPE MOSFET:**

Depletion-type MOSFETs are further classified as

(i) N-channel D-type MOSFET  
(ii) P-Channel D-type MOSFET

**N-CHANNEL DEPLETION TYPE MOSFET:**

The basic construction of the n-channel depletion type MOSFET is as shown in fig (10). A slab of p-type material is formed from a Si base and is referred to as the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions linked by a n-channel. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin SiO₂ layer. The presence of SiO₂ layer accounts for very high input impedance of the device. The input impedance of MOSFET is higher than JFET.
Fig 10: Construction n-Channel Depletion type MOSFET.

A small n layer is implanted in the region below SiO₂ to create n-channel. The insulating layer between gate and the channel has resulted in another name for the device: Insulated-gate FET or IGFET.

OPERATION OF N-CHANNEL DEPLETION MODE MOSFET:

Case i: $V_{GS} = 0$ and $V_{DS} = +ve$ voltage
Since drain is positive with respect to source, the free electrons are attracted from source to drain to constitute drain current $I_D$. The drain characteristics and transfer characteristics of depletion mode MOSFET is as shown in fig 11.

Case ii: $V_{GS} = -ve$ Voltage and $V_{DS} = +ve$ small voltage
The negative potential at the gate will cause the electrons to move towards p-type substrate as charges repel while holes from p-type substrate are attracted toward gate. Depending on the magnitude of negative bias established by $V_{GS}$, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, higher is the rate of recombination. The resulting level of $I_D$ is reduced with the increasing levels of negative bias for $V_{GS}$ as in fig11.
Case iii: $V_{GS} = +ve$ Voltage and $V_{DS} = +ve$ small voltage

For positive values of $V_{GS}$, the +ve gate will draw additional electrons from p-type substrate as minority charge carriers are attracted towards gate. New carriers are generated due to collisions and $I_D$ will increase at a rapid rate. Thus, application of $+V_{GS}$ has enhanced the level of free carriers in the channel compared to $V_{GS} = 0V$. The region of +ve gate voltage on the drain or transfer characteristics is referred as enhancement region. The region between the cut-off and the saturation level of $I_{DSS}$ is refereed as the depletion region.

Transfer characteristics are a plot of $I_D$ as a function of $V_{GS}$ with $V_{DS}$ as constant. Shockley Equation as in equation 2 is used to plot transfer characteristics.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Also, Short hand method can be used to plot transfer characteristics curve.

Condition1: $V_{GS} = 0$, Hence from eq(2),
\[ I_D = I_{DSS}. \]

Condition 2: \( V_{GS} = V_P \)

Therefore from equation 2 \( I_D = 0 \text{mA}. \)

Condition 3: \( V_{GS} = \frac{V_P}{2} \)

Therefore from equation 2, \( I_D = I_{DSS}/4 \)

Condition 4: \( I_D = I_{DSS}/2 \)

From eq(1), \[ V_{GS} = V_P(1 - \sqrt{I_D/I_{DSS}}) \]

\[ V_{GS} = V_P(1 - \sqrt{0.5}) \]
\[ V_{GS} = 0.3V_P \]
\[ V_{GS} = 0.3V_P \]

Points are marked for these conditions of \( V_{GS} \) and \( I_D \) and the co-ordinates are joined using smooth curve.

**P-CHANNEL DEPLETION TYPE MOSFET:**

The basic construction of the p-channel depletion type MOSFET is as shown in fig (12a). A slab of n-type material is formed from a Si base and is referred to as the substrate. The source and drain terminals are connected through metallic contacts to p-doped regions linked by a p-channel. The gate is also connected to a metal contact surface but remains insulated from the p-channel by a very thin SiO\(_2\) layer. The presence of SiO\(_2\) layer accounts for very high input impedance of the device. The input impedance of MOSFET is higher than JFET.
Fig 12: (a) Construction   (b) Transfer Characteristics   (c) Drain characteristics

OPERATION OF P-CHANNEL DEPLETION MODE MOSFET:

Case i: $V_{GS} = 0$ and $V_{DS} = -$ve voltage
Since drain is negative with respect to source, the holes are attracted from source to drain to constitute drain current $I_D$. The drain characteristics and transfer characteristics of depletion mode MOSFET is as shown in fig 12(c) and (b) respectively.

Case ii: $V_{GS} =$ +ve Voltage and $V_{DS} =$ -ve small voltage
The positive potential at the gate will cause the holes to move towards n-type substrate as charges repel while electrons from n-type substrate are attracted toward gate. Depending on the magnitude of positive bias established by $V_{GS}$, a level of recombination between electrons and holes will occur that will reduce the number of holes in the p-channel available for conduction. The more positive the bias, higher is the rate of recombination. The resulting level of $I_D$ is reduced with the increasing levels or positive bias for $V_{GS}$ as in fig12(c).

Case iii: $V_{GS} =$ -ve Voltage and $V_{DS} =$ -ve small voltage
For positive values of $V_{GS}$, the -ve gate will draw additional holes from n-type substrate as minority charge carriers are attracted towards gate. New carriers are generated due to
collisions and $I_D$ will increase at a rapid rate. Thus, application of $-V_{GS}$ has enhanced the level of free carriers in the channel compared to $V_{GS} = 0V$.

Transfer characteristics are a plot of $I_D$ as a function of $V_{GS}$ with $V_{DS}$ as constant. Shockley Equation as in equation 2 is used to plot transfer characteristics.

\[ I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \]

Also, Short hand method can be used to plot transfer characteristics curve.

Condition 1: $V_{GS} = 0$, Hence from eq(3),

\[ I_D = I_{DSS} \]

Condition 2: $V_{GS} = V_P$

Therefore from equation 2 $I_D = 0mA$.

Condition 3: $V_{GS} = V_P/2$

Therefore from equation 2,$ID = I_{DSS} \left( 1 - \frac{1}{2} \right)^2$

\[ I_D = I_{DSS}/4 \]

Condition 4: $I_D = I_{DSS}/2$

From eq(1) $VGS = VP \left( 1 - \sqrt{ID/I_{DSS}} \right)$

\[ VGS = VP \left( 1 - \sqrt{0.5} \right) \]
\[ VGS = 0.3VP \]
\[ VGS = 0.3VP \]

Points are marked for these conditions of $V_{GS}$ and $I_D$ and the co-ordinates are joined using smooth curve.

**SYMBOLS OF DEPLETION TYPE MOSFET**

Fig 13 shows the symbols of n-channel and p-channel Depletion mode MOSFET.
N-CHANNEL ENHANCEMENT-MODE MOSFET (E-MOSFET):
The construction of n-channel enhancement mode MOSFET is as shown in fig 14. The starting material is a p-type substrate into which highly doped n-regions are diffused to form source and drain regions. A layer of SiO₂ is grown allover the p-type substrate and is etched to create window for n-diffusion. The source and drain terminals are taken out through metallic contacts to n-doped regions as shown in fig 14. Metal is deposited on SiO₂ to create Gate. The presence of SiO₂ between gate and p-substrate provides electrical isolation between the two regions. No channel exists between source and drain in E-MOSFET.

Fig 14: Construction of n-channel E-MOSFET

OPERATION OF N-CHANNEL E-MOSFET:

Case i: $V_{GS} = 0$ and $V_{DS} = +ve$ voltage
The application of drain to source voltage while gate and source are shorted will cause no ID to flow as no channel exists for this condition.

**Case ii: \( V_{GS} = +ve \) Voltage and \( V_{DS} = +ve \) small voltage**

When gate is made positive with respect to source, electrons are attracted towards the gate but holes are repelled back into p-type substrate. Since the region under the gate is p-type substrate, the positive voltage on gate causes holes which are majority charge carriers in p-type substrate to repel and move towards substrate. A positive \( V_{GS} \) and positive \( V_{DS} \) causes the two pn junctions to be reverse biased and depletion region is formed. Now the device is said to be in depletion mode. The positive \( V_{GS} \) also causes electrons to be attracted towards the gate. Now, device is said to be in accumulation mode. Since the region below the gate was p-substrate and accumulation of electrons has caused the type to change to n-type. Thus the device is said to be in inversion mode as shown in fig 15. A positive \( V_{GS} \) has caused a thin layer of negative charge to be formed in the substrate under the gate. Thus, channel is said to be created. The value of \( V_{GS} \) which causes channel to be formed under the gate is called threshold voltage (\( V_T \)). A small ID flows. When \( V_{GS} \) is increased above \( V_T \), conductivity of the channel is enhanced and thus pulling more electrons into the channel. When \( V_{GS} < V_T \), there is no channel. Since channel is formed by the application of \(+V_{GS}\), the type of MOSFET is Enhancement type. As \( V_{GS} \) is increased further, higher level of ID flows as shown in fig 16. A positive \( V_{GS} \) cause potential drop across the channel. For large \( V_{DS} \) this voltage may not be sufficient to invert the channel near the drain end there by causing drain current to saturate. The channel is said to be pinched off. ID flows due to diffusion.

![Fig 15: Formation of Inversion layer](image-url)

**TRANSFER CHARACTERISTICS OF N-CHANNELE-MOSFET:**

The transfer characteristics of n-channel E-MOSFET is as shown in fig 16. For \( V_{GS} > V_T \), the relationship between drain current and \( V_{GS} \) is nonlinear and is given by eqn 4.

\[
ID = K(V_{GS} - V_T)^2 \quad \text{----------Eq 4}
\]

Where \( K \) is a constant and is a function of the construction of the device as given by Eqn 5.

\[
K = \frac{ID(ON)}{(V_{GS(ON)} - V_T)^2} \quad \text{----------Eq 5}
\]
Thus $I_D$ increases steadily when $V_{GS} > V_T$ and $I_D$ is zero when $V_{GS} < V_T$.

**p-CHANNELEnhancement-Mode MOSFET (E-MOSFET):**
The construction of p-channel E-MOSFET is opposite to that of n-channel E-MOSFET. Substrate is of n-type and source, drain are of p-type as in fig 17(a). The voltage polarities and current directions are reversed in p-channel E-MOSFET. The drain and transfer characteristics of p-channel E-MOSFET are as shown in Fig 17 (c) and (b) respectively.

**OPERATION OF P-CHANNEL E-MOSFET:**
Case i: $V_{GS} = 0$ and $V_{DS} = -ve$ voltage

The application of drain to source voltage while gate and source are shorted will cause no ID to flow as no channel exists for this condition.

Case ii: $V_{GS} = -ve$ Voltage and $V_{DS} = -ve$ small voltage

When gate is made negative with respect to source, holes are attracted towards the gate but electrons are repelled back into n-type substrate. Since the region under the gate is n-type substrate, the negative voltage on gate causes electrons which are majority charge carriers in n-type substrate to repel and move towards substrate. A negative $V_{GS}$ and negative $V_{DS}$ causes the two pn junctions to be reverse biased and depletion region is formed. Now the device is said to be in depletion mode. The negative $V_{GS}$ also causes holes to be attracted towards the gate. Now, device is said to be in accumulation mode. Since the region below the gate was n-substrate and accumulation of holes has caused the type to change to p-type. Thus the device is said to be in inversion mode. A negative $V_{GS}$ has caused a thin layer of positive charges to be formed in the substrate under the gate. Thus, channel is said to be created. The value of $V_{GS}$ which causes channel to be formed under the gate is called threshold voltage ($V_{T}$). A small ID flows. When $V_{GS}$ is decreased below $V_{T}$, conductivity of the channel is enhanced and thus pulling more electrons into the channel. When $V_{GS} > V_{T}$, there is no channel. Since channel is formed by the application of $-V_{GS}$, the type of MOSFET is Enhancement type. The drain characteristics are as shown in fig 17 (c).

TRANSFER CHARACTERISTICS OF P-CHANNEL E-MOSFET:

The $V_{GS}$ is negative and $I_{D}$ flows in opposite direction. The transfer characteristics of p-channel E-MOSFET is as shown in fig 17(b). $I_{D}$ increases steadily with $V_{GS}$.

E-MOSFET SYMBOLS:

Fig 18 (a) and 18(b) shows the symbols of n-channel and p-channel E-MOSFET.

FET CONFIGURATION:
The three types of FET configuration are:

(i) Common Source (CS) Configuration  
(ii) Common Drain (CD) Configuration  
(iii) Common Gate (CG) Configuration

**FET BIASING:**
Biasing is done to establish proper levels of DC voltages and currents for desired region of operation. It establishes Q-point.

**TYPES OF BIASING:**

(i) Fixed Bias  
(ii) Self Bias  
(iii) Voltage divider Bias

Voltage divider bias most widely used biasing technique in amplifiers.

**FET AS AN AMPLIFIER:**

Fig. 19 Shows Common Source Circuit. The Voltage $V_{GG}$ provides the necessary reverse-bias between gate and source of JFET. The signal to be amplified is $V_S$. The transfer Characteristics of JFET is as shown in Fig. 20. A DC load line is drawn on the characteristics. The point of intersection of DC load line on Transfer characteristics for specific $V_{GS}$ is called Q-point. Let Q point be situated at the middle of DC load line.

![Fig 19: CS Amplifier with Fixed Bias](image1) ![Fig 20: Locate Q-Point](image2)

The instantaneous $V_{gs}$ is

$V_{gs}=V_S-V_{GG}$  \[ (6) \]

Both $I_D$ and $V_{DS}$ can be considered as sinusoid superimposed on the DC values.
Then \( V_{GS} = V_{GG} + V_{gs} \)  ---- (7)

\[ I_D = I_d + I_{DQ} \]

\[ V_{OUT} = V_{DS} = V_{DSQ} + V_{ds} \]  ---- (8)

Since output signal is greater than input signal, amplification has occurred. The magnitude of Voltage gain is the ratio of output voltage to input voltage.

\[ |AV| = \frac{V_o}{V_s} \]

The selection of Q point at the middle gives undistorted output. If the operating point is located either closer to ohmic region or near pinch-off voltage, the output waveform will be clipped during +Ve or –Ve half cycles. In Common Source circuit, output is 180° out of phase with input.

To locate Q point, the following procedure is used

- Plot transfer characteristics
- Draw a vertical line (load line) from \( V_{GS} = -V_{GG} \).
- Intersection of load line with transfer characteristics will give Q point.

Fig 20 shows the position of Q point using the above procedure.

**JFET parameters**

**Transconductance:** The change in the Drain Current due to change in Gate to Source voltage is defined as Transconductance ‘\( g_m \).

\[ g_m = \frac{\Delta I_D}{\Delta V_{GS}} \]

We know that, \( I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \)  ---- (9)

And \( g_m = \frac{\Delta I_D}{\Delta V_{GS}} \)

Differentiate Eq. (9) w.r.t \( V_{GS} \)

\[ \frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS} \times 2 \left( 1 - \frac{V_{GS}}{V_P} \right) \left( - \frac{1}{V_P} \right) \]

\[ g_m = -2 \frac{I_{DSS}}{V_P} \left( 1 - \frac{V_{GS}}{V_P} \right) \]  ---- (10)

Also from Eq. (9) \[ 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{l_D}{l_{DSS}}} \]  ---- (11)

Therefore substitute Eq. (11) in Eq. (10),

we get, \[ g_m = -2 \frac{l_{DSS}}{V_P} \sqrt{\frac{l_D}{l_{DSS}}} = -\frac{2}{V_P} \sqrt{\frac{l_D l_{DSS}^2}{l_{DSS}}} \]

therefore \[ g_m = -\frac{2}{V_P} \sqrt{l_D l_{DSS}} \]  ---- (12)

when \( V_{GS} = 0 \), \( g_m = g_{m0} \)

therefore from Eq. (10), \[ g_{m0} = -\frac{2l_{DSS}}{V_P} \]  ---- (13)

Substitute Eq. (13) in Eq. (10)

we get, \[ g_m = g_{m0} \left( 1 - \frac{V_{GS}}{V_P} \right) \]
Drain Resistance, \( r_d \): The ratio of change in Drain to Source voltage to change in Drain current is called Drain resistance, \( r_d \) with constant \( V_{GS} \).

\[
\frac{\Delta V_{DS}}{\Delta I_D} = V_{GS=\text{constant}}
\]

\( r_d \) determines the output impedance \( Z_O \) of the JFET amplifier.

**JFET small signal model:**

Fig. (21) shows low frequency small signal model for n-channel JFET. The relationship between \( I_D \) and \( V_{GS} \) is

\[
\Delta I_D = g_m \Delta V_{gs}
\]

and hence a current Source is connected from Drain to Source. The input impedance of JFET is high and hence \( I_G=0 \). Thus in the small signal model input impedance is represented by open circuit. The output impedance is represented by \( r_d \) from Drain to Source.

![Fig. (21) n-JFET small signal model](image)

Approximate model

Since \( r_d \gg \) external Drain resistance \( R_D \), \( r_d \) can be replaced by open circuit as shown in Fig. (22).

![Fig. (22) Approximate small signal model of n-JFET.](image)
COMMON SOURCE (CS) AMPLIFIER WITH FIXED BIASING:

Fig 23: CS Amplifier with Fixed Bias
Fig 24: DC equivalent Circuit

Fig 23 shows CS amplifier with fixed bias. RG is used to limit current in case VGG is connected with wrong polarity. This would forward bias the gate-source junction causing high currents, which would destroy the transistor.

DC Analysis:

Open circuit C₁ & C₂ and current through RG i.e. IG=0. Therefore RG is represented by short circuits as shown in Fig. (24).

Apply KVL to the input circuit of Fig. (24)
VGG-VGS=0
VGS=-VGG ----- (14)
Since VGG is constant, VGS is fixed and hence the name fixed bias.

Apply KVL to output circuit
VDD-IDRD-VDS=0
VDSQ=VDD-IDRD ----- (15)
And ID for fixed bias is IDQ= IDSS\left(1 - \frac{VGS}{VP}\right)^2
Therefore Q point is \([VDS, IDQ]\)

Small signal analysis:

(i) To obtain AC equivalent circuit, short circuit C₁, C₂ and reduce DC voltages to zero.
(ii) Replace JFET by its small signal model to obtain AC equivalent circuit Fig. (25).

![AC equivalent circuit diagram]

**Fig 25: ac equivalent circuit**

\[ \text{Z}_i: \text{From the circuit, Fig. (25)} \]
\[ \text{Z}_i= R_G \]
\[ \text{Z}_o: \]
\[ \text{Reduce } V_i=0, V_{gs}=0 \text{ therefore } g_m V_{gs}=0. \]
\[ Z_o=R_D || r_d \]
\[ \text{If } r_d>> R_D, \text{ Then } Z_o=R_D \]
\[ \text{Voltage gain, } A_V: \]
\[ A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i} \]

From Fig. (25) \[ V_o = - g_m V_{gs} (r_d || R_D) \text{ and } V_i=V_{gs} \]
\[ A_V = - g_m V_{gs} (r_d || R_D) \]

If \( r_d >> R_D \), \[ A_V = - g_m R_D \]

The negative sign indicates there is a phase shift of 180° between input and output voltages.

**COMMON SOURCE (CS) AMPLIFIER WITH SELF BIAS:**

Fig 26 shows Common Source amplifier with self bias. Voltage across RS determines gate to source voltage. Dc equivalent circuit is obtained by open circuiting all capacitors as shown in fig 27.

Apply KVL to Fig27,
\[-V_{GS} - V_S = 0 \]
\[V_S = -V_{GS}. \]
Also, \[ V_S = I_D R_S \]
Therefore, \[ V_{GS} = -I_D R_S \]

Apply KVL to output circuit of fig27,
\[ V_{DS} = V_{DD} - I_D R_S - I_D R_D \]
Fig 26. CS amplifier with Self Bias

Fig 27 DC equivalent Circuit

Fig 28: Q point

Fig 8 shows the location of Q point obtained by following procedure.

- Plot transfer characteristics
- Plot one point of load line at $V_{GS} = 0$, $I_D = 0$.
- Second point can be obtained by choosing $I_D$ and finding $V_{GS}$.
- $I_D = I_{DSS}/2$, then

$$V_{GS} = -I_D R_S = -I_{DSS} R_S / 2$$

Join two points to draw DC load line

- Intersection of load line with transfer characteristics will give Q point.

**CS amplifier with Self Bias (Bypassed Rs) – ac analysis**
Fig 29 shows CS amplifier with Self bias and RS is bypassed by CS. Fig 30 shows ac equivalent Circuit obtained by short circuiting C1,C2,CS.

Replacing JFET by its equivalent small signal model results in circuit shown in Fig 31.

Fig 31: AC equivalent model of CS amplifier with Self bias

- **Zi:** From the circuit, Fig. (31)
  
  \[ Z_i = R_G \]

- **Zo:**
  
  Reduce \( V_i = 0 \), \( V_{gs} = 0 \) therefore \( g_m V_{gs} = 0 \).

  \[ Z_o = R_D || r_d \]

  If \( r_d >> R_D \), Then \( Z_o = R_D \)

- **Voltage gain, \( A_V \):**
  
  \[ A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{gs}} \]

  From Fig. (31) \( V_o = - g_m V_{gs} (r_d || R_D) \) and \( V_i = V_{gs} \)

  \[ A_V = - g_m V_{gs} (r_d || R_D) \]

  If \( r_d >> R_D \), \( A_V = - g_m R_D \)

  The negative sign indicates there is a phase shift of \( 180^\circ \) between input and output voltages.
**CS amplifier with Self Bias (UnBypassedRs) – ac analysis**

Fig 32 shows CS amplifier with self bias but RS is unbypassed. To obtain ac equivalent circuit, c1 and c2 are short circuited as shown in Fig 33. Replacing JFET by its equivalent small signal model, we get the circuit shown in Fig 34.

![CS amplifier with self bias](image)

**Fig 32: CS amplifier with self bias**

![Ac Equivalent Circuit](image)

**Fig 33: ac Equivalent Circuit**

![Ac Equivalent model](image)

**Fig 34: ac Equivalent model**

Zi: From Fig 34,

\[ Z_i = R_G. \]
Zo’: Output impedance excluding RD.

\[ Z_{o'} = V_o / I_d \]

Apply KVL to the output circuit of Fig 34,

\[ V_o = I_1 r_d + I_d R_S \]

But, \( I_1 = I_d g_m V_{gs} \).

Therefore, \( V_o = (I_d - g_m V_{gs}) + I_d R_S \) ---------------(16)

Apply KVL to the input circuit of Fig 34,

\[ V_i - V_{gs} - I_d R_S = 0 \]

\[ V_{gs} = -I_d R_S + V_i \]

For output impedance, \( V_i = 0 \).

Therefore, \( V_{gs} = -I_d R_S \) ---------------------------(17)

Substituting Eq (17) in (16)

\[ V_o = I_d (r_d + g_m R_S r_d + R_S) \]

Therefore, \( Z_{o'} = V_o / I_d = r_d + g_m R_S r_d + R_S \)

But, \( \mu = g_m r_d \)

Therefore, \( Z_{o'} = r_d + R_s (\mu + 1) \) --------------------------(18)

Thus, output impedance with unbypassed RS is increased.

Zo: Output impedance considering RD

\[ Z_o = Z_{o'} || R_D \]

Voltage Gain ,AV:

From Fig 34, \( V_o = -I_d R_D \) -----------------------------(19)

Apply KVL to the outer part of Fig 34,

\[ (I_d - g_m V_{gs}) r_d + I_d R_D + I_d R_S = 0; \] ---------------(20)

Also \( V_{gs} = V_i - I_d R_S \) --------------------------(21)

Eq (21) in Eq (20)

\[ I_d = (g_m V_i r_d) / (r_d + g_m R_S r_d + R_s + R_D) \] -----------(22)

Eq (22) in Eq (19)

\[ V_o = (-g_m V_i r_d R_D) / (r_d + g_m R_S r_d + R_s + R_D) \]

\[ A_V = V_o / V_i = -g_m r_d R_D / r_d + g_m R_S r_d + R_s + R_D \]

If \( r_d >> R_s + R_D \),

\[ A_V = -g_m R_D / (1 + g_m R_S) \]

Example: For the CS amplifier shown, operating point is defined by \( V_{GSQ} = -2.5V, V_P = -6V \) and \( I_{DQ} = 2.5mA \) with \( I_{DSS} = 8mA \). Calculate \( g_m, r_d, Z_i, Z_o \) and \( A_V \). Take \( Y_{os} = 20 \mu S \)

\[ g_m = g_{mo} \left( 1 - \frac{V_{GS}}{V_P} \right) \]
\[ g_{\text{mo}} = \frac{2I_DSS}{V_P} = \frac{2 \times 8 \times 10^{-3}}{6} = 2.67 \text{mS} \]

\[ g_m = g_{\text{mo}} \left(1 - \frac{V_{GS}}{V_P} \right) = \left(1 - \frac{(-2.5V)}{(-6V)} \right) = 1.58 \text{mS} \]

(ii) \[ r_d = \frac{1}{y_{OS}} = \frac{1}{20 \times 10^{-6}} = 50 \text{K}\Omega \]

(iii) \[ Z_i = R_G = 1 \text{M}\Omega \]

(iv) \[ Z_o = Z_o' || R_D = r_d + R_S(\mu +) || R_D = 2163.41 \Omega \]

(v) \[ A_V = \frac{V_o}{V_i} = -g_m r_d R_D / r_d + g_m R_S r_d + R_S + R_D = \text{1.315}. \]

**CS amplifier with Voltage Divider Bias (Bypassed Rs):**

Fig 35 Shows voltage divider bias circuit.

DC analysis: Open circuit C1, C2, CS and the resultant circuit is as shown in Fig 36.
From Fig 36,

\[ V_G = V_{DD} \left( \frac{R_2}{R_1 + R_2} \right) \]

\[-V_G + V_{GS} + I_D R_S = 0\]

\[ V_{GS} = V_G - I_D R_S \]

\[ V_{DS} = V_{DD} - I_D \left( R_D + R_S \right) \]

Fig 37 shows the procedure to fix Q point in voltage divider bias.

Fig 37: Fixing Q Point.
AC Analysis: AC Equivalent Circuit is obtained by Shorting C1, C2 and CS as shown in Fig 38. Replacing JFET by its small signal model, we get the circuit shown in Fig 39.

![AC Equivalent Circuit](image1)

**Fig 38: AC Equivalent Circuit**

![AC Equivalent model](image2)

**Fig 39: AC Equivalent model**

- **Zi**: From the circuit, Fig. (39)
  \[ Z_i = R_1 || R_2 \]
- **Zo**:
  Reduce \( V_i = 0 \), \( V_{gs} = 0 \) therefore \( g_m V_{gs} = 0 \).
  \[ Z_o = R_D || r_d \]
  If \( r_d >> R_D \), Then \( Z_o = R_D \)

- **Voltage gain, \( A_V \)**:
  \[ A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i} \]
  From Fig. (39) \( V_o = - g_m V_{gs} (r_d || R_D) \) and \( V_i = V_{gs} \)
  \[ A_V = - g_m V_{gs} (r_d || R_D) \]
  If \( r_d >> R_D \), \( A_V = - g_m R_D \)

The negative sign indicates there is a phase shift of 180° between input and output voltages.

**CS amplifier with Voltage Divider Bias (UnBypassed Rs): ac Analysis**

Fig 40 Shows CS voltage divider bias with un-bypassed RS. AC Analysis is obtained by short circuiting C1,C2 and the resultant circuit is shown in Fig 41. Replacing JFET by its equivalent small signal model, we get circuit shown in Fig 42.
Zi: From Fig 42,

\[ Z_i = R_1 || R_2. \]

Zo’: Output impedance excluding RD.

\[ Z_o' = \frac{V_o}{I_d} \]

Apply KVL to the output circuit of Fig 42,

\[ V_o = I_r R_d + I_d R_S \]

But, \( I_1 = I_d g_m V_{gs} \).

Therefore, \( V_o = (I_d g_m V_{gs}) + I_d R_S \) \[\text{(23)}\]

Apply KVL to the input circuit of Fig 42,

\[ V_i - V_{gs} - I_d R_S = 0 \]
\[ V_{gs} = -I_dR_S + V_i \]

For output impedance, \( V_i = 0 \).
Therefore, \( V_{gs} = -I_dR_S \) ---------------(24)

Substituting Eq (24) in (23)
\[ V_0 = I_d(r_d + g_mR_Sr_d + R_S) \]
Therefore, \( Z_0' = \frac{V_0}{I_d} = r_d + g_mR_Sr_d + R_S \)
But, \( \mu = g_mr_d \)
Therefore, \( Z_0' = r_d + R_S(\mu + 1) \) ---------------(25)

Thus, output impedance with unbypassed RS is increased.

\[ Z_0: Output \ impedance \ considering \ RD \]
\[ Z_0 = Z_0'||R_D \]

Voltage Gain, \( A_V \):
From Fig 42, \( V_o = -I_dR_D \) --------------------------(26)

Apply KVL to the outer part of Fig 42,
\( (I_d - g_mV_{gs})r_d + I_dR_D + I_dR_S = 0; \) ---------------(27)

Also \( V_{gs} = V_i - I_dR_S \) --------------------------(28)

Eq (27) in Eq (26)
\[ I_d = \frac{(g_mV_i)r_d}{(r_d + g_mR_Sr_d + R_S + R_D)} \]--------------------------(29)

Eq (22) in Eq (19)
\[ V_o = \frac{(-g_mV_iR_D)}{(r_d + g_mR_Sr_d + R_S + R_D)} \]
\[ A_V = \frac{V_o}{V_i} = \frac{-g_mR_D}{(r_d + g_mR_Sr_d + R_S + R_D)} \]

If \( r_d >> R_S + R_D \),
\[ A_V = \frac{-g_mR_D}{(1 + g_mR_S)} \]

**Common Drain (CD)/ Source Follower Configuration:**

Fig. (43) shows Common Drain configuration. The input is applied between Gate and Source and output between Source and Ground (i.e. Drain is grounded during AC analysis)

![Source Follower Circuit](image)

From the circuit in Fig 43,
\[ V_G + V_{GS} - V_S = 0 \]
Therefore \( V_G + V_{GS} = V_S \)
When a signal is applied to JFET gate via \( C_1 \), \( V_G \) varies with the signal. As \( V_{GS} \) is constant and \( V_S = V_G + V_{GS} \) varies with \( V_i \). As the output voltage at the Source (\( V_S \))
follows changes in the signal voltage applied to the gate, this circuit is also called Source follower.

The AC equivalent circuit and low frequency equivalent model for Source follower is as shown in Fig. (44) and Fig. (45) respectively.

![AC Equivalent Circuit](image)

**Fig. (44) AC Equivalent Circuit**

![AC Equivalent Model](image)

**Fig. (45) AC Equivalent Model**

\[ V_i - V_{gs} - V_o = 0 \]
\[ V_o = V_i - V_{gs} \]
\[ V_o + V_{gs} - V_i = 0 \]
\[ V_{gs} = V_i - V_o \]
\[ V_i = 0, V_{gs} = -V_o \]

**Z_i:**
From the input circuit,
\[ Z_i = R_G \]

**Output Z:** \[ Z_o \]
Fig. (45) can also be written as Fig. (46)
\[ Z_o = \frac{V_o}{I_d} \]

Apply KVL to the output loop of Fig 46,
\[ V_i - V_{gs} - V_o = 0 \]
For \[ Z_o \], \[ V_i = 0, V_o = V_{gs} \]
But from Fig. (46), \[ I_d = g_m V_{gs} \]
Therefore \( g_m V_o = I_d \)
\[
\dot{Z}_o \text{=} \frac{V_o}{I_d} = \frac{1}{g_m}
\]
Therefore \( Z_o = \dot{Z}_o \parallel R_S \)
\[
Z_o = \frac{1}{g_m} + R_S
\]
**Voltage Gain, \( A_V \)**
\[
A_V = \frac{V_o}{V_i}
\]
From Fig. (46),
\[
V_o = I_d (r_d \parallel R_S)
\]
And \( I_d = g_m V_{gs} \)
Therefore \( V_o = g_m V_{gs} (r_d \parallel R_S) \)
From input circuit
\[
V_i = -V_{gs} + V_o
\]
Therefore \( V_i = -g_m V_{gs} (r_d \parallel R_S) - V_{gs} \)
Therefore \( A_V = \frac{\frac{V_o}{V_i}}{-g_m V_{gs} (r_d \parallel R_S)} = \frac{-g_m V_{gs} (r_d \parallel R_S)}{-V_{gs} [g_m (r_d \parallel R_S) + 1]} \)
\[
A_V = \frac{g_m (r_d \parallel R_S)}{1 + g_m (r_d \parallel R_S)}
\]
If \( r_d \gg R_S \), \( r_d \parallel R_S \approx R_S \)
\[
A_V = \frac{g_m R_S}{1 + g_m R_S}
\]
If \( g_m R_S >> 1 \), \( A_V \approx 1 \) but it is always less than one.
There is no phase shift between input and output voltages.
Source Follower exhibits following Characteristics;

- High input Impedance.
- Low Output Impedance
- Voltage gain is less than 1.
- No phase shift between input and output.

Example: A DC analysis of Source Follower network shown in Fig. below results in \( V_{GSQ} = -2.86V \) and \( I_{DQ} = 4.56mA \). Determine (i) \( g_m \) (ii) \( r_d \) (iii) \( Z_i \) (iv) \( Z_o \) with and without \( r_d \) (v) \( A_V \) with and without \( r_d \). Take \( I_{DSS} = 16mA \), \( V_P = -4V \), \( Y_{OS} = 25\mu S \).
(i) \[ g_{mo} = \frac{2I_{DSS}}{V_P} = \frac{2 \times 16 \times 10^{-3}}{4} = 8 \text{mS} \]
\[ g_m = g_{mo} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = 8 \times 10^{-3} \left( 1 - \frac{(-2.86)}{(-4)} \right) \]
\[ g_m = 2.28 \times 10^{-3} \text{S}. \]

(ii) \[ r_d = \frac{1}{V_{OS}} = \frac{1}{25 \times 10^{-6}} = 40 \text{K} \Omega \]

(iii) \[ Z = R_G = 1 \text{M} \Omega \]

(iv) With \( r_d \)
\[ Z_0 = r_d R_S \frac{1}{g_m} = 40 \text{K} \parallel 2.2 \text{K} \frac{1}{2.28 \times 10^{-3}} \]
\[ = 362.52 \Omega \]
Without \( r_d \)
\[ Z_0 = R_S \parallel \frac{1}{g_m} = 2.2 \times 10^3 \frac{1}{2.28 \times 10^{-3}} \]
\[ = 365.69 \Omega \]

(v) \[ A_V = \frac{g_m(r_d \parallel R_S)}{1 + g_m(r_d \parallel R_S)} = 0.826. \]
\[ A_V \] Without \( r_d \)
\[ A_V = \frac{g_m R_S}{1 + g_m R_S} = \frac{2.28 \times 10^{-3} \times 2.2 \times 10^3}{1 + 2.28 \times 10^{-3} \times 2.2 \times 10^3} = 0.833 \]

**Common Gate (CG) Configuration:**

Fig. (47) shows CG configuration, the input is applied between Source and Gate and output is taken between Drain and Gate.

![Common Gate Configuration Diagram](image-url)
increase in output $V_g$. Similarly when input $V_g$ reduces, opposite action takes place which reduces the output voltage. Thus there is no phase shift between input and output in a Common Gate amplifier. AC equivalent model of CG amplifier is as shown in Fig. (48).

![AC Equivalent Model](image1)

![AC Equivalent Model Redrawn](image2)

\[ \dot{Z}_i = \frac{V_i}{I} \]

Current through $r_d$ (Fig 49)

\[ I_{id} = I + g_m V_{gs} \]

Therefore \[ I = I_{id} - g_m V_{gs} ------ (30) \]

From the circuit,

\[ I_{id} = \frac{V_i - lR_D}{r_d} ------ (31) \]

Substitute Eq. (31) in Eq. (30)

\[ I = \frac{V_i - lR_D}{r_d} - g_m V_{gs} ------ (32) \]

But $V_i = -V_{gs}$ (from Fig. (49))

Therefore \[ I = \frac{V_i - lR_D}{r_d} + g_m V_i \]

\[ I = \frac{V_i}{r_d} - \frac{lR_D}{r_d} + g_m V_i \]

\[ I \left[ 1 + \frac{R_D}{r_d} \right] = V_i \left[ \frac{1}{r_d} + g_m \right] \]

\[ V_i = \frac{1}{l} + \frac{r_d}{r_d + g_m} = \frac{r_d + R_D}{g_m r_d + 1} = \dot{Z}_i \]

\[ Z_i = \dot{Z}_i \left| R_S = R_S \left| \frac{r_d + R_D}{1 + g_m r_d} \right. \right. \]

If $r_d \gg R_D$ and $g_m r_d \gg 1$,

\[ Z_i = R_S \left| \frac{r_d}{g_m r_d} = R_S \parallel \frac{1}{g_m} \right. \]

Input impedance of CG amplifier is less than CS and CD amplifier.

\[ Z_o : \text{when } V_i = 0 \text{ i.e. when input is short circuited, the equivalent circuit is} \]

\[ Z_o = r_d \parallel R_D \]

If $r_d \gg R_D$, $Z_o \approx R_D$

\[ A_v = \frac{V_o}{V_i} \]
V_o = I_D R_D and V_i = -V_{gs}

Apply KVL to Fig. (b) outer loop

V_i + (I_d - g_m V_{gs})r_d + I_D R_D = 0

But V_{gs} = v_i

Therefore V_i + I_d r_d + g_m V_i r_d + I_D R_D = 0

V_i [1+g_m r_d] + I_d [r_d + R_D] = 0

-I_d [r_d + R_D] = V_i [1+g_m r_d]

V_i = \frac{-I_d (r_d + R_D)}{1+g_m r_d}

A_V = \frac{V_o}{V_i} = \frac{R_D (1+g_m r_d)}{r_d + R_D}

If \ r_d \gg R_D, \ g_m r_d >> 1

A_V = \frac{R_D (g_m r_d)}{r_d} = R_D g_m

Thus there is no phase shift between input and output in CG amplifier.

Example: For the network shown, if V_{GSQ} = -2.2V and I_{DQ} = 2.03mA. Determine g_m, r_d.

Calculate Z_i with and without r_d, Z_o with and without r_d. Determine v_o with and without r_d.

(i) \ g_{mo} = \frac{2 I_D S}{V_p} = \frac{2 \times 10 \times 10^{-3}}{4} = 5 \text{mS}

\ g_m = g_{mo} \left(1 - \frac{V_{GSQ}}{V_p}\right) = 5 \times 10^{-3} \left(1 - \frac{(-2.2)}{(-4)}\right)

\ g_m = 2.25 \times 10^{-3} \text{S.}

(ii) \ r_d = \frac{1}{Y_{OS}} = \frac{1}{50 \times 10^{-6}} = 20 \text{K}\Omega

(iii) \ \frac{r_d + R_D}{g_m r_d + 1} = \mathcal{Z}_t = 0.31 \text{K}\Omega

(iv) \ \mathcal{Z}_t = \mathcal{Z}_i \| R_S = R_S \| \frac{r_d + R_D}{1+g_m r_d} = 0.35 \text{K}\Omega

(v) \ Z_o \approx R_D = 3.6 \text{K}\Omega

(vi) \ Z_o = r_d \| R_D = 3.05 \text{K}\Omega
(vii) \( A_V R_D g_m = 8.1 \)

(viii) \( A_V \frac{V_o}{V_i} = \frac{R_D (1 + g_m r_d)}{r_d + R_D} = 7.02 \)

(ix) \( v_o \text{ without } r_d = 324mV \)

\( v_o = 280.8mV \)